Interfacing QDR^{TM}-II SRAM with Stratix^{TM}, Stratix II and Stratix GX Devices

AN4064

Introduction

Synchronous static RAM (SRAM) architectures are evolving to support the highthroughput requirements of communications, networking, and digital signal processing (DSP) systems. The successor to Quad Data Rate™ (QDR™) SRAM, QDR-II SRAM supports higher memory bandwidth and improved timing margin and offers more flexibility in system designs.

QDR-II SRAM provides more than four times the bandwidth of other SRAM architectures. Most SRAM solutions are designed for PCs and have interfaces that move data efficiently for long bursts of read or write operations. In contrast, most communications applications require data transfer between the SRAM and the memory controller that alternates between read and write cycles. Devices with bidirectional interfaces, such as standard synchronous pipelined SRAM devices, do not perform well in these applications.

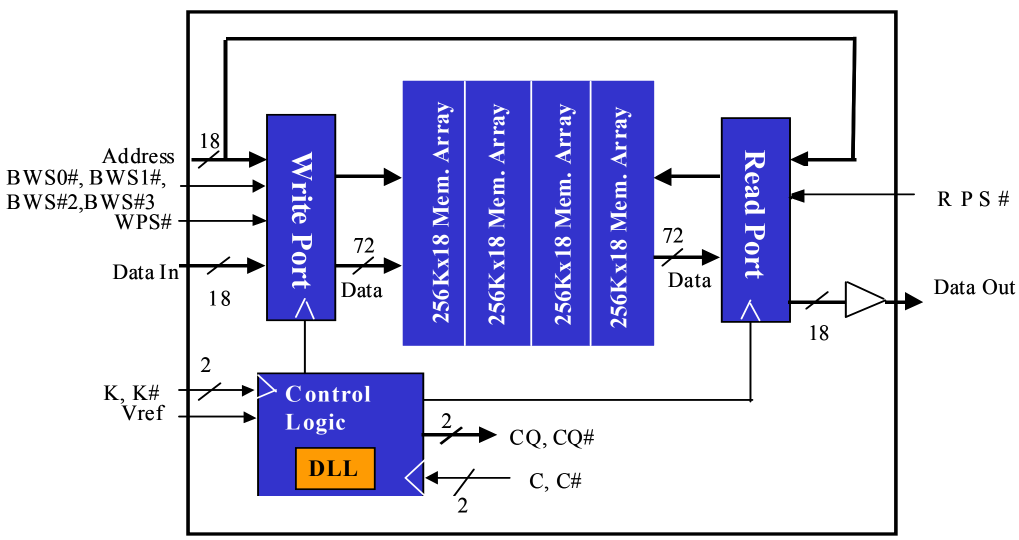
Cypress, along with the other QDR consortium members, defined the QDR-II SRAM architecture for high-performance communications systems. The QDR-II SRAM devices from these companies are pin-compatible.

QDR-II SRAM devices provide concurrent read and write operations and increased data throughput, allowing simultaneous access to the same address location. This innovative architecture outperforms other SRAM devices by up to four times in networking applications, where read and write operations are balanced.

This application note describes a system that interfaces a QDR-II SRAM memory device with a Stratix, Stratix II, or Stratix GX FPGA. It provides details on timing analysis for the interface with the FPGA.

Use this application note together with the External Memory Interfaces chapter of the *Stratix II Device Handbook* or the *Stratix Device Handbook*. For more information on QDR-II SRAM devices, go to www.cypress.com

Figure 1. 18-Mbit QDR-II SRAM Burst-of-4 Architecture.



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QDR-II SRAM Functional Description

QDR-II SRAM can perform two data writes and two data reads per clock cycle. It uses one port for writing data (D) and another port for reading data (Q). These unidirectional data ports support simultaneous reads and writes and allow back-to-back transactions without the bus contention issues that may occur when using a single bidirectional data bus. Write and read operations share the address bus. QDR-II SRAM devices use three pairs of clocks: Input Clocks K and Kn (controlling the input signals), output clocks C and Cn (controlling the output data bus), and echo clocks CQ and CQn (source synchronous clocks).

QDR-II SRAM devices use either the 1.5V-HSTL or 1.8V-HSTL Class I/II I/O standard. Cypress recommends using the 1.8-HSTL Class I I/O standard for maximum performance in Stratix II devices. Either 1.8V or 1.5V HSTL can be used in Stratix and Stratix GX devices. Write and read operations are burst-oriented and support burst lengths of two and four, so each read and write operation transfers either two or four data words. QDR-II SRAM performs write operations the same way as QDR SRAM. However, read operations in QDR-II SRAM output the data half a clock cycle later than QDR SRAM to improve the clock to output time (tCO).

Figure 1 shows a block diagram of the QDR-II SRAM burst-of-4 architecture.

QDR-II SRAM Functionality

Both burst-of-2 and burst-of-4 devices provide the same overall bandwidth at a given clock speed. This section describes the functionalities of burst-of-2 and burst-of-4 QDR-II SRAM devices.

Burst-of-2 QDR-II SRAM Devices

Burst-of-2 QDR-II SRAM devices support two-word data transfers on all write and read transactions, requiring a relatively simple controller implementation. This section outlines the basic burst-of-2 functionality for write-only, read-only, and combined read/write operations, assuming the K and Kn clocks are used for both reads and writes, and the C and Cn clocks are connected to VDD(Device is in Single Clock Mode).

Figure 2 shows the burst-of-2 timing diagram for reads and writes. The sizes of the Address, Data-In, and Data-Out buses depend on the memory device with which the FPGA interfaces.The BWSn signal is low for the entire cycle of Figure 2.

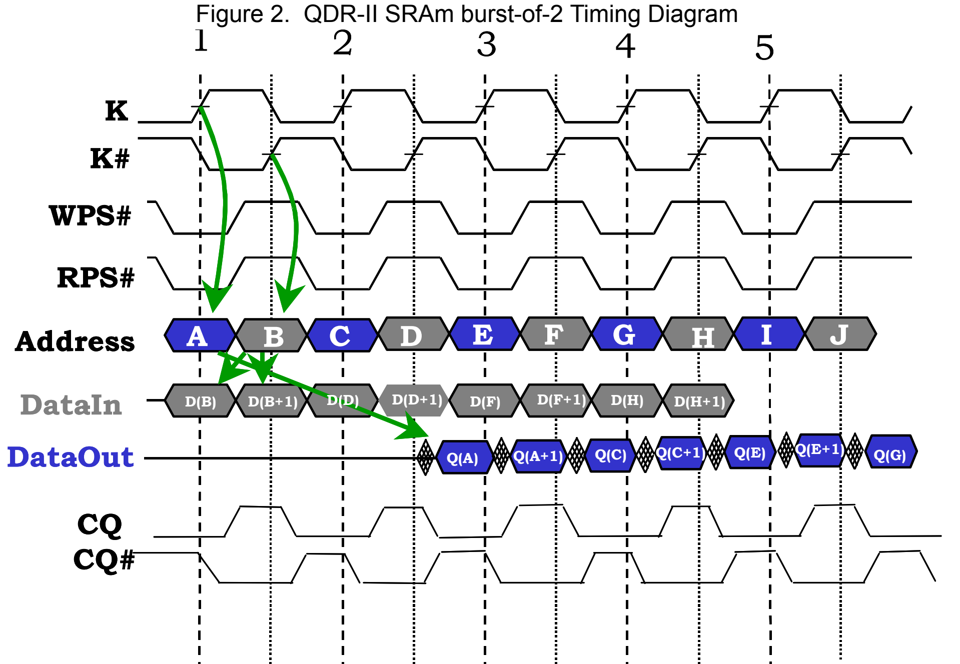
Write Cycle

On the rising edge of the K clock, the QDR-II SRAM device latches the control signals WPSn and BWSn and the lower data word on Data-In (D[A] at Cycle 1 of Figure 2). On the rising edge of the Kn clock, the QDR-II SRAM device latches the write address on B (Cycle 1 in Figure 2) and the upper data word (D[B + 1]) on Data-In, thus completing a write cycle.

Read Cycle

On the rising edge of the K clock, the QDR-II SRAM device latches the control signal RPSn and the read address A (Cycle 1 of Figure 2). After a one-and-a-half-clock-cycle latency, the rising edge of Kn clocks out the lower data word (Q[A]) of address A onto the Data-Out bus. The QDR-II SRAM device outputs the upper data word (Q[A + 1]) on the next rising edge of the K signal, completing the read cycle.

Figure 2. QDR-II SRAm burst-of-2 Timing Diagram



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Read/Write Cycle

Read and write operations occur during the same clock cycle on independent read and write datapaths along with the cycle-shared address bus. Performing concurrent reads and writes does not change the functionality of either transaction. If a read request occurs simultaneously with a write request at the same address, the data on Data-In is forwarded to Data-Out. Therefore, latency is not required to access valid data.

Burst-of-4 QDR-II SRAM Devices

Burst-of-4 QDR-II SRAM devices support four-word data transfers on all writes and reads, which reduces address bus activity. However, the control circuitry needed to interface to burst-of-4 QDR-II SRAM devices is more complicated than control circuitry for burst-of-2 QDR-II SRAM devices. The following sections outline the basic burst-of-4 functionality for writes, reads, and read/write operations, assuming the K and Kn clocks are used for both read and write operations and the C and Cn clocks are connected to VDD (device is in Single Clock Mode).

Figure 3 shows the burst-of-4 timing diagram for alternating reads and writes. The sizes of the Address, Data-In, and Data-Out buses depend on the memory device with which the FPGA interfaces. The BWSn signal is low for the entire cycle of Figure 3.

Write Cycle

The QDR-II SRAM device latches the control signals WPSn and BWSn and the write address A (A at Cycle 1 of Figure 3) on the rising edge of the K clock. On the following K clock rising edge, the QDR-II SRAM device latches the first data word (D[A]) on Data-In. On the next Kn clock rising edge, the second data word is latched (D[A + 1]). The third (D[A + 2]) and fourth (D[A + 3]) words are latched in on the subsequent K and Kn clock rising edges, respectively, completing a write cycle.

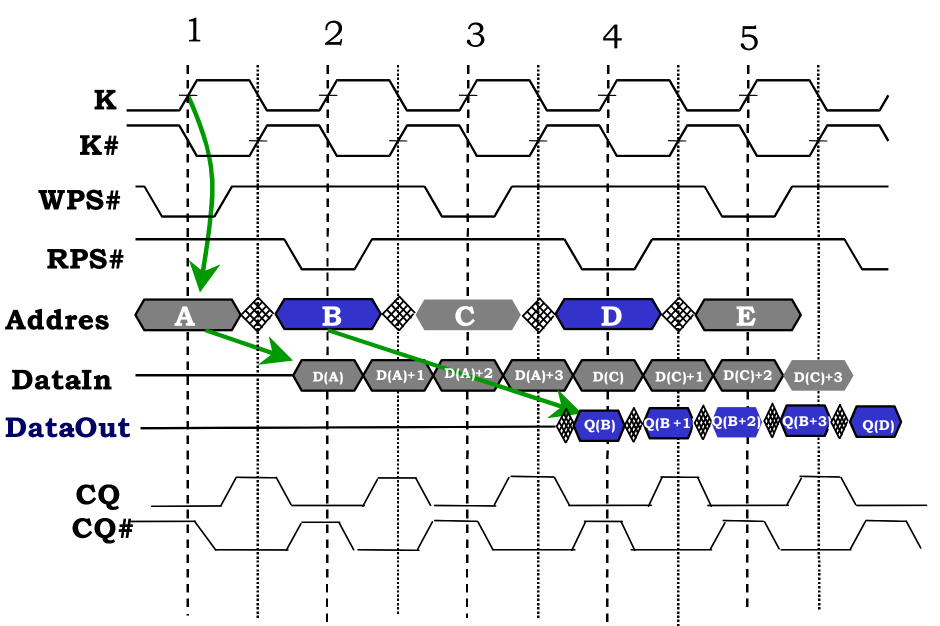
Read Cycle

The QDR-II SRAM device latches the control signal RPSn and the read address B (Cycle 2 in Figure 3) on the rising edge of the K clock. After a one-and-a-half-clock-cycle latency, the rising edge of Kn clocks out the first data word (Q[B]) of address B onto the Data-Out bus. The next rising edge of K clocks out the second data word (Q[B + 1]). The subsequent rising edges of Kn and K clock out the third (Q[B + 2]) and fourth (Q[B + 3]) words, respectively, completing a read cycle. Single-clock mode uses the K and Kn clocks for both reads and writes.

Read/Write Cycle

Read and write operations occur on subsequent clock cycles on the independent read and write datapaths along with the cycle-shared address bus. Performing concurrent reads and writes does not change the functionality of either transaction. If a read request occurs simultaneously with a write request at the same address, the data on Data-In is forwarded to Data-Out. Therefore, latency is not required to access valid data.

Figure 3. QDR-II SRAM Burst-of-4 Timing Diagram



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QDR-II SRAM Interface Signals

This section provides a description of the clock, control, address, and data signals on a QDR-II SRAM device. Table 1 shows the QDR-II SRAM interface pins and how to connect them to Stratix II, Stratix, and Statix GX devices.

When interfacing with one QDR-II SRAM device, Stratix II, Stratix, and Stratix GX devices use a single-clock scheme where the QDR-II SRAM device's C or Cn port is tied to VDD(Single Clock Mode).

Table 1. QDR-II SRAM Interface Pins

Pins	Description	Stratix II Pin Utilization for QDR-II SRAM	Stratix and Stratix GX Pin Utilization for QDR-II SRAM
D	Write Data	User I/O pin	User I/O pin
Q	Read Data	DQ	DQ
K	Write Clock	User I/O pin	User I/O pin
Kn	Inverted Write Clock	User I/O pin	User I/O pin
C	Read Clock	N/A	N/A
Cn	Inverted Read Clock	N/A	N/A
CQ	Echo Clock	DQS	PLL Dedicated Clock Input
CQn	Inverted Echo Clock	DQSn	Not Used
All Other	Address and Command	User I/O pin	User I/O pin

Clock Signals

QDR-II SRAM devices have three pairs of clocks:

- Input clocks K and Kn
- Output clocks C and Cn
- Echo clocks CQ and CQn.

The positive input clock, K, is the logical complement of the negative input clock, Kn. Similarly, C and CQ are complements of Cn and CQn, respectively. The QDR-II SRAM device uses the K and Kn clocks for write accesses and the C and Cn clocks for read accesses. CQ and CQn are the source synchronous output clocks from the QDR-II SRAM device to accompany the read data.

The number of loads that the K and Kn clocks drive affects the switching times of these outputs. When a controller drives a single QDR-II SRAM device, C and Cn are unnecessary because the propagation delays from the controller to the QDR-II SRAM device and back are the same. To reduce the number of loads on the clock traces, QDR-II SRAM devices also have a single-clock mode, where the K and Kn clocks are used for both reads and writes. The QDR-II SRAM device still uses CQ and CQn for the echo clock from the memory device to the Stratix II device. In this mode, the C and Cn clocks are tied to the supply voltage (VDD)(Device is in Single Clock Mode).

The Stratix II, Stratix, or Stratix GX device outputs the K and Kn clocks and the data, address, and command lines to the QDR-II SRAM device. For the controller to operate properly, the write data (D), address (A), and control signal trace lengths (and the propagation times) should be approximatly equal to the K and Kn clock trace lengths. Since the propagation delays for K and Kn from the FPGA to the QDR-II SRAM device are equal to the delays on the data and address (D and A) signals, the signal skew effect on the write and read request operations is minimized. This delay matching is achieved by using identical double date rate output circuits to generate the clock and data inputs to the memory.

The QDR-II SRAM device generates echo clocks CQ and CQn, which are edge-aligned with the leading edge of the read data. The CQ and CQn signals are then phase-shifted inside the Stratix II, Stratix, or Stratix GX device and used to capture the read data. The CQ and CQn signal board trace length between the QDR-II SRAM device and the controller should be equal to the read data (Q) board trace length to minimize the skew between the two signals.

For Stratix II interfaces to QDR-II memories, connect the CQ and CQn pins to the FPGA DQS and DQSn pins, respectively. Both phase-shifted CQ and CQn signals are used to capture the read data. The CQ pin is connected to the input latch and the active-high input register, while the CQn pin is connected to the active-low input register.

For best data alignment, invert the CQ and CQn signals before they arrive at the DQ IOE registers. You can select this option in the altdq megafunction. See the External Memory Interfaces chapter of the *Stratix II Device Handbook* for more information.(http://www.altera.com/literature/hb/stx2/stratix2_handbook.pdf Volume 2 Chapter 3).

For Stratix and Stratix GX interfaces to QDR-II memories, connect the CQ echo clock pin to the dedicated reference input clock pin of the FPGA phase-locked loop (PLL). The CQn pin is not used, as the PLL can only use one reference clock. The PLL is used to phase-shift the CQ signal and used tand ground pins for better noise immunity.

Use regular I/O pins in Stratix II I/O banks 3, 4, 7, or 8 via the double data rate (DDR) registers to generate the K and Kn clocks. To meet the QDR-II tKHKH (skew between K and Kn) requirement, use adjacent pins for the complementary signals and surround the pin-pair with programmable VCC and ground pins for better noise immunity.

Data Signals

QDR-II SRAM devices use two unidirectional data buses, one for writes (D) and one for reads (Q). Connect Q to the DQ pins on the Stratix II, Stratix, or Stratix GX FPGA. You can connect any of the FPGA user I/O pins in I/O banks 3, 4, 7 or 8 to the D ports.

Control Signals

QDR-II SRAM devices use the write port select (WPSn) signal to control write operations and the read port select (RPSn) signal to control read operations. The byte write select signal (BWSn) is a third control signal that tells the QDR-II SRAM device which byte to write into the QDR-II SRAM device. You can use any of the FPGA user I/O pins in I/O banks 3, 4, 7 or 8 to generate the control signals.

Address Signals

QDR-II SRAM devices use one address bus (A) for both read and write addresses. You can use any of the FPGA user I/O pins in I/O banks 3, 4, 7 or 8 to generate the address signals.

QDR-II SRAM Interface Architecture

The QDR-II SRAM interface architecture in Stratix II FPGAs has minor differences when compared to the Stratix and Stratix GX architecture. This difference exists in the read implementation. Stratix and Stratix GX FPGAs use a read PLL to center align the CQ echo clock with the read data (Q). A PLL is used instead of the delay-locked loop (DLL) since it has better phase shift granularity in Stratix and Stratix GX FPGAs. In Stratix II FPGAs, however, the enhanced DLL and delay shift circuitry are used to center align the echo clocks (CQ and CQn) with read data (Q).

The write implementation is identical. A write PLL is used to generate the write data (D) and center aligned system clocks (K and Kn) using the dedicated DDR I/O circuits. This implementation results in matched propogation delays for clock and data signals from the FPGA to the QDR-II SRAM, minimizing skew.

Datapath Architecture in Stratix II

The QDR-II implementation in Stratix II uses two PLLs:

- A write PLL to generate K/Kn system clocks and clock out address, command, and data.
- A read DLL-based phase shift circuitry to register read data from the memory using echo clocks CQ/CQn.

Figure 4 depicts the Stratix II memory interface datapath architecture. Specifically, it shows how to connect the clocks, data, address, and control pins in Stratix II devices when interfacing with QDR-II SRAM devices. The write PLL generates two clock outputs, WRITE_CLK and WRITE_CLK_90, that have a 90° phase offset. The WRITE_CLK output is used to clock out the address, command, and data signals to the QDR-II SRAM, while the WRITE_CLK_90 output is used to generate the K/Kn memory input clocks. This architecture centrally aligns the K and Kn write clock edges to the output data (D) and address (A) signals. All outputs to the memory (including the clock) use the double -data rate registers or DDIO circuitry in the IO cell, significantly minimizing the skew between clock and data channels.

The read DQS phase shift circuitry generates a centrally aligned version of CQ and CQn echo clocks for read data capture. The example in Figure 4 uses a feedback clock (FB_CLK) and a second PLL for resynchronization. The FB_CLK clock feeds a PLL whose output clocks the resynchronization register. Without any PLL shifting, the output of this PLL is aligned with the unshifted CQ and can be used for resynchronization without calculating the round trip delay (RTD) of the system. The board trace length for the feedback clock FB_CLK should be the same as the signal board trace lengths for CQ or CQn, which is equal to l2 in Figure 4.

If the Stratix II write PLL input clock and the QDR-II SRAM frequencies are different, you must provide the input reference clock to the DQS phase shift circuitry either from another input clock pin or from PLL 5 or 6. See the External Memory Interfaces Chapter from the *Stratix II Handbook* for more information.(http://www.altera.com/literature/hb/stx2/stratix2_handbook.pdf Volume 2 Chapter 3).

The feedback clock, FB_CLK, can be tapped from the K clock, as shown in Figure 4. You can also use an extra pin to generate the feedback clock, and the FB_CLK pin is fed back to the read PLL input pin. The board trace length for this feedback loop should be equal to l1 + l2. This removes any extra skew due to a loading mismatch between K and Kn. However, you need to account for skew between K or Kn and FB_CLK in the resynchronization timing analysis.The input reference clock can either be from the input_clk, another clock pin, or the PLL 5 or 6 output.

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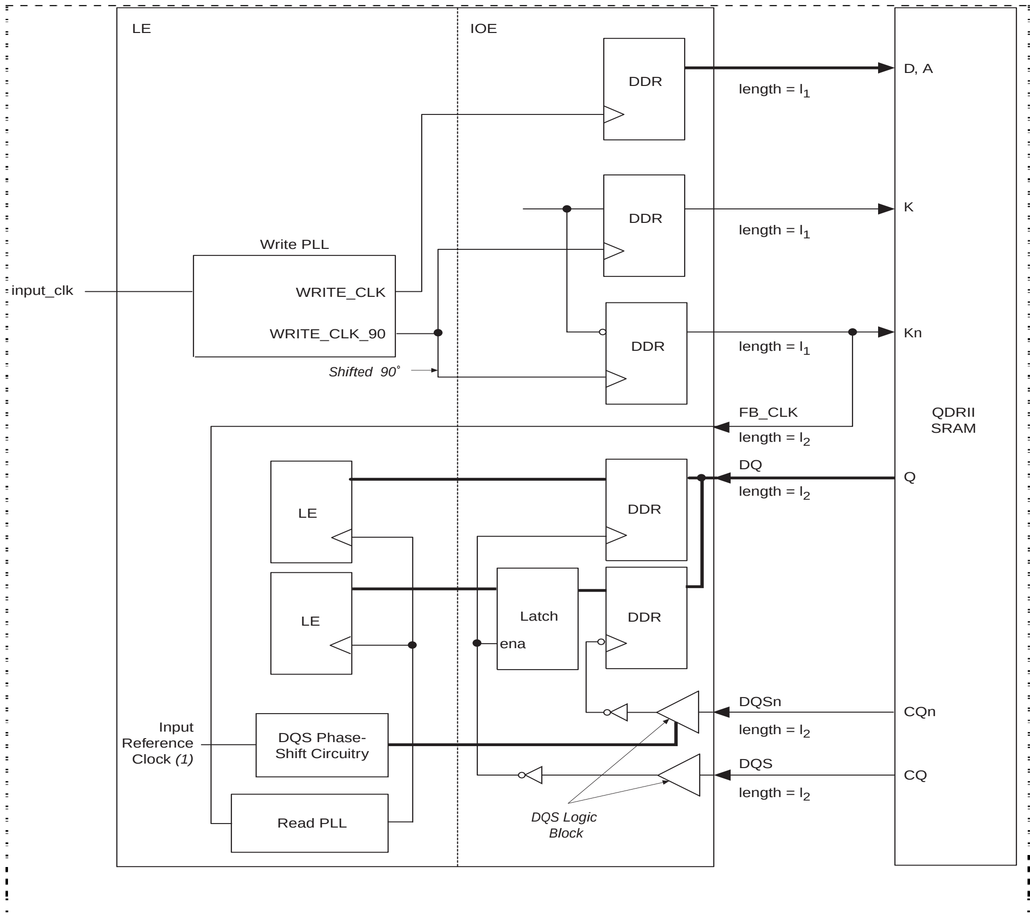
Figure 4. QDR-II SRAM Interface Datapath in Stratix II FPGAs.



Datapath Architecture in Stratix and Stratix GX

The QDR-II implementation in Stratix uses two PLLs:

- A write PLL to generate K/Kn system clocks and clock out address, command, and data
- A read PLL to register data from memory using echo clocks CQ/CQn.

Figure 5 shows the datapath implementation in Stratix and Stratix GX devices. The write PLL generates two clock outputs, WRITE_CLK and WRITE_CLK_90, that have a 90-degree phase offset. The WRITE_CLK output is used to clock out the address, command, and data signals to the QDR-II SRAM, while the WRITE_CLK_90 output is used to generate the K/Kn memory input clocks. This architecture centrally aligns the K and Kn write clock edges to the output data (D) and address (A) signals. All outputs to the memory (including the clock) use the double data rate registers or DDIO circuitry in the IO cell, significantly minimizing the skew between clock and data channels.

The read PLL generates a phase-shifted version of the CQ echo clock to capture read data (Q) signals.

Timing Analysis

Since data is transferred between the FPGA memory controller and the QDR-II SRAM device at high speeds, it is essential to make sure to avoid set-up or hold violations for the QDR-II SRAM and the FPGA. This section illustrates the timing analysis that must be performed when designing a high-speed QDR-II SRAM interface.

Write Cycle Timing

It is essential to meet the QDR-II SRAM device set-up and hold requirements for correct write cycle timing. For example, the data set-up and hold specifications for the Cypress burst-of-4 250-MHz devices are 0.35 ns each. And they are 0.4 ns each for the Cypress burst-of-4 200-MHz devices.

The FPGA controller drives both the QDR-II SRAM clock and data signals. Therefore, the clock-to-output delay from the

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FPGA are almost identical for both sets of pins. The board delays for the clock and data are assumed to be equal because the signal trace lengths are matched. Because K and Kn are generated from the WRITE_CLK_90 signal, while data and address are generated from the WRITE_CLOCK signal, there is a timing margin of approximatly one-half of the bit period (the length of time between each data bit) each way to meet the QDR-II SRAM device set-up and hold times. The bit period, by definition, is approximatly one-half of the cycle time for double data rate signaling.

Figure 6 shows the write cycle timing waveform for the QDR-II SRAM interface pins for Stratix II.

In addition to set-up and hold times, an additional concern is the clock-to-clock skew between K and Kn (tKHKH). The 250-MHz QDR-II SRAM specification allows for up to 0.2 ns difference between the rising edges of the K and Kn signals. Because Stratix II device clock-to-out times can vary with pin position, K and Kn need to be placed on adjacent pins and their tCO times need to be verified to meet this requirement. Preliminary timing shows that the controller meets the tKHKH specification when the K and Kn pins are adjacent. For better noise immunity, surround the pin pair with programmable VDD and ground pins.

In the following exercise, we analyze the timing for a write operation from a Stratix EP1S40 device to a Cypress CY7C1313AV18-200 burst-of-4 QDR-II SRAM device. We will analyze timing for a 200-MHz interface.

Let us start the timing analysis by studying the input clocks K and Kn. These clocks are generated by the WRITE_CLK_90 output of the PLL inside the FPGA. The data, address, and command outputs are clocked out by a different output of the same PLL. Since two outputs of a PLL feeding global clock networks have an inherent skew, the K and Kn clocks could be offset from the data outputs by this amount. For the Stratix Enhanced PLLs, skew between two PLL outputs using different counters is 150 ps. This specification is listed in the DC and Switching Characteristics chapter in the *Stratix and Stratix GX Device Handbook* (Volume 1 Chapter 4).

Figure 7 illustrates this and other uncertainties on the clock and data signals.

Figure 5. QDR-II Datapath Architecture in Stratix andStratix GX FPGAs

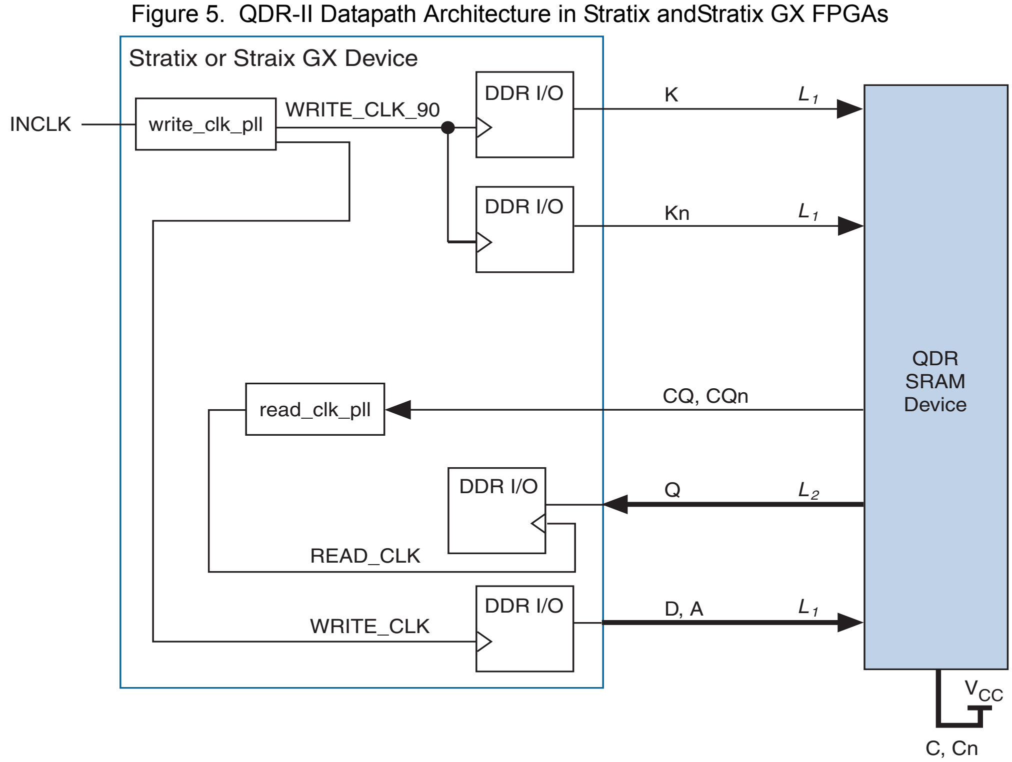

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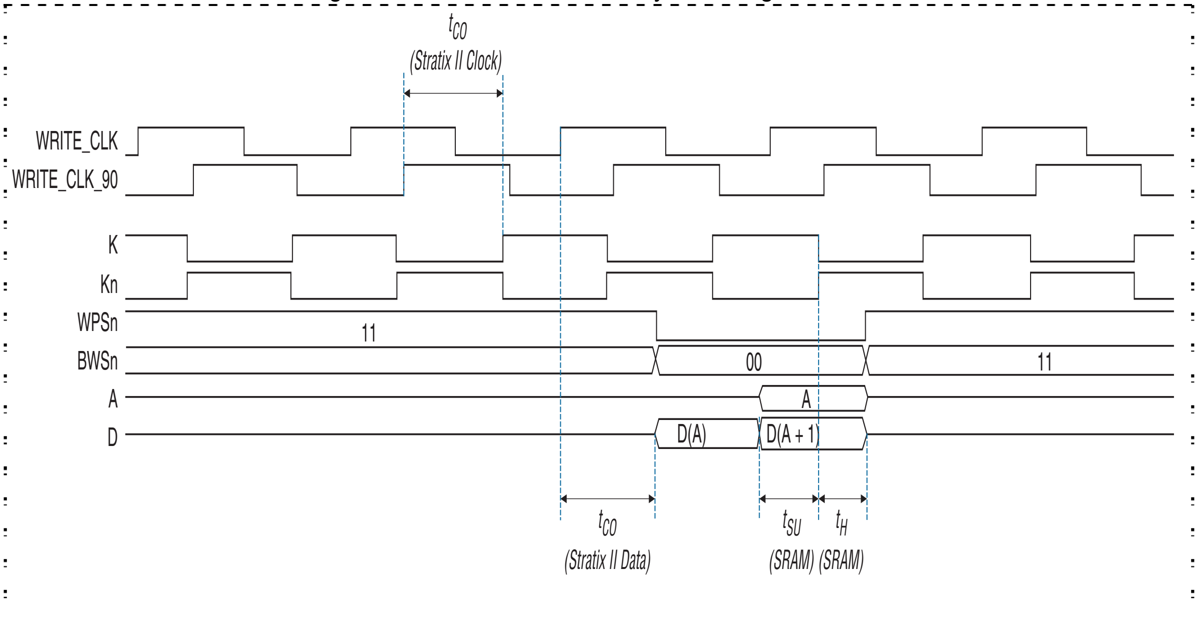
Figure 6. QDR-II SRAM Write Cycle Timing Waveform



This results in a minimum phase offset between these two clocks:

tSHIFT_MIN = (0.25 * clock period) - clock skew = 0.25 * 5 – 0.15 = 1.1 ns

Similarly, the maximum phase offset between the two PLL output clocks:

tSHIFT_MAX = (0.25 * clock period) + clock skew = 0.25 * 5 ns + 0.15 = 1.4 ns

In addition to this clock skew uncertainty, PLL outputs can have duty cycle distortion (DCD) up to ±5% of the clock period. This results in an additional clock uncertainty of ± 250 ps (±5% of 200-MHz clock). Another source of uncertainty on the clock is PLL jitter. However, since PLL jitter affects both the clock and data outputs to the memory uniformly, it does not affect the set-up/hold relationship on the QDR-II SRAM.

In Figure 7, the ideal clock edge of WRITE_CLK_90 is expected at time t=3750 ps. After accounting for PLL output clock skew and duty cycle distortion, the clock edge can occur anytime between t=3350 ps and t=4150 ps.

Next, we compute the uncertainties on the data (D) signals. Channel-to-channel skew amongst all data pins is equal to the worst-case skew between the DDR outputs within the I/O bank(s). When using a single column I/O bank in the EP1S40 devices, the worst-case skew is Tio_skew = ± 290 ps. Additionally, board trace length variations could add to this channel-to-channel skew. While this implementation calls for perfectly matched trace lengths, the timing analysis allows for ± 50 ps of board skew. These skew parameters affect the data valid window on the QDR-II memory. FPGA I/O skew and board skew can reduce the data valid window on the QDR-II SRAM by 680 ps.

Now that the uncertainties are established, we check the set-up and hold time margins for write operations at the memory input pins. For a 200-MHz operation, the bit period is (5.0 ns / 2) = 2.5 ns. The Cypress QDR-II SRAM device has set-up and hold time requirements of 400 ps at this speed.

Given these parameters, the set-up and hold margins for 200-MHz QDR-II in Stratix are as follows:

Set-up time margin is the least when the data arrives late and the clock arrives early. Set-up time margin is calculated as:

tsu_margin = tSHIFT_MIN – tDS – tDCD – tIO_SKEW = 1.1 – 0.4 – 0.250 – 0.290 = 0.110 ns

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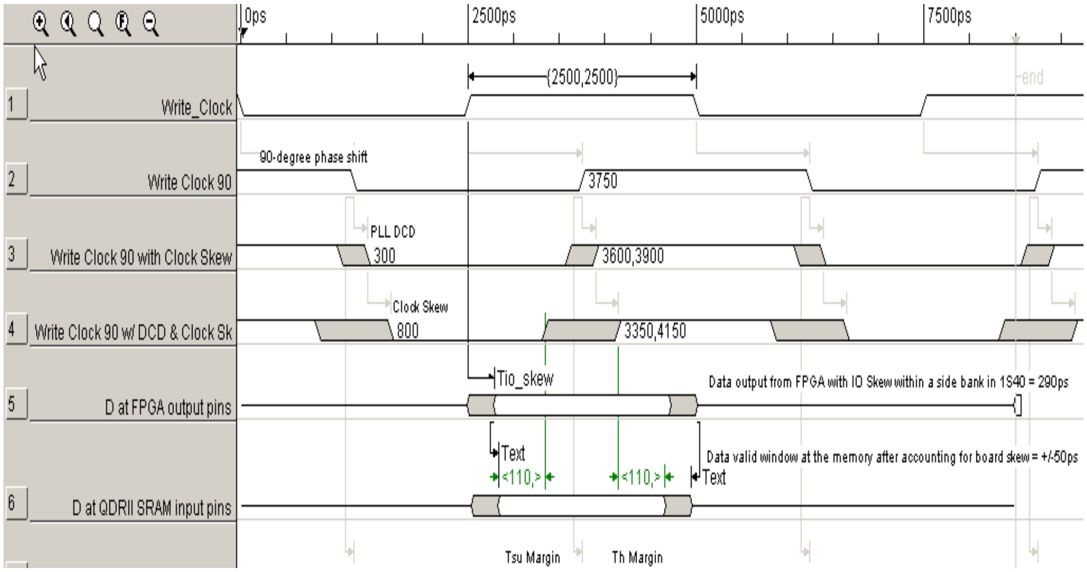
Figure 7. QDR-II SRAM Write Timing Waveform: Uncertainties and Margins



Hold time margin is the least when the data arrives early and clock arrives late. The margin is calculated as:

tH_margin = tck / 2 – tSHIFT_MAX – tDS – tDCD – tIO_SKEW = 2.5 – 1.4 – 0.4 – 0.250 – 0.290 = 0.110 ns

The total margin available is the sum of the set-up and hold margins = 0.220 ps.

Table 2 and Table 3 show the QDR-II SRAM timing margin calculations for write operations when the board trace variations for the D and K/Kn pins are 50 ps (approximately 0.3” of FR4 trace length variations). Table 2 shows timing margins for a Stratix II EP2S60 interfacing with 200-MHz and 250-MHz QDR-II SRAMs, while Table 3 shows timing margins for a Stratix EP1S40 FPGA interfacing with 167-MHz and 200-MHz QDR-II SRAMs. A similar timing analysis for other interfaces with a different FPGA and QDR-II SRAM device combination by replacing timing specifications from the corresponding data sheets.

Table 2. Example Stratix II EP2S60 QDR-II SRAM Write Timing Analysis

	Specification	200 MHz (ps)	250 MHz (ps)	Description
	t_{CYC}	5000	4000	Clock Period
Memory Spec	t_{DS}=t_{DH}	400	350	Data (D) set-up and hold time from the memory data sheet = 0.4 ns and 0.35 ns, respectively Address (A) set-up and hold time from the memory data sheet = 0.6 ns and 0.5 ns, respectively
FPGA Spec	t_{IOSKEW}	160	160	Absolute value of the difference in clock-to-out times (tCO) between any two output registers on the top and bottom of the device fed by a common clock source
	$t_{CLKSKEW}$	150	150	Skew between two PLL outputs
	t_{DCD}	250	200	Duty cycle distortion (5% of clock period)
	t_{JITTER}	0	0	Data and clock outputs from FPGA are generated the same PLL and jitter together, thus canceling one another.
Board Spec	t_{EXT}	50	50	Board trace variations for the D, Q, and clock lines (166-ps per inch for an FR4 trace)
Calculation	t_{SHIFT_MIN}	1100	850	Minimum shift from the PLL (0.25*t_{CK} (90° shift) – $t_{CLKSKEW}$)
	t_{SHIFT_MAX}	1400	1150	Maximum shift from the PLL (0.25*t_{CK} (90° shift) + $t_{CLKSKEW}$)

Table 2. Example Stratix II EP2S60 QDR-II SRAM Write Timing Analysis (Continued)

	Specification	200 MHz (ps)	250 MHz (ps)	Description
Result	Data Valid Window @ QDR-II	1280	880	$0.5*t_{CK} – 2*(t_{DCD} + t_{IOSKEW} + t_{EXT} + t_{CLKSKEW})$
	Write set-up Timing Margin	240	90	$t_{SHIFT\_MIN} – t_{DCD} – t_{IOSKEW} – t_{EXT} – t_{DS}$
	Write Hold Timing Margin	240	90	$0.5*t_{CK} – t_{SHIFT\_MAX} – t_{DCD} – t_{IOSKEW} – t_{EXT} – t_{DH}$
	Total Margin	480	180	$0.5*t_{CK} – t_{DH} – t_{DS} – 2*(t_{DCD} + t_{IOSKEW} + t_{EXT} + t_{CLKSKEW})$

Table 3. Example Stratix EP1S40 QDR-II SRAM Write Timing Analysis

	Specification	167 MHz (ps)	200 MHz (ps)	Description
	t_{CYC}	6000	5000	Clock Period
Memory Spec	$t_{DS}=t_{DH}$	500	400	Data (D) set-up and hold time from the memory data sheet = 0.5 ns and 0.4 ns, respectively Address (A) set-up and hold time from the memory data sheet = 0.7 ns and 0.6 ns, respectively
FPGA Spec	t_{IOSKEW}	290	290	Absolute value of the difference in clock-to-out times (tCO) between any two output registers on the top and bottom of the device fed by a common clock source
	$t_{CLKSKEW}$	150	150	Skew between two PLL outputs
	t_{DCD}	300	250	Duty cycle distortion (5% of clock period)
	t_{JITTER}	0	0	Data and clock outputs from FPGA are generated the same PLL and jitter together, thus canceling one another.
Board Spec	t_{EXT}	50	50	Board trace variations for the D, Q, and clock lines (166-ps per inch for an FR4 trace)
Calculation	t_{SHIFT_MIN}	1350	1100	Minimum shift from the PLL ($0.25*t_{CK}$ (90° shift) – $t_{CLKSKEW}$)
	t_{SHIFT_MAX}	1650	1400	Maximum shift from the PLL ($0.25*t_{CK}$ (90° shift) + $t_{CLKSKEW}$)
Result	Data Valid Window @ QDR-II	1420	1020	$0.5*t_{CK} - 2*(t_{DCD} + t_{IOSKEW} + t_{EXT} + t_{CLKSKEW})$
	Write set-upTiming Margin	210	110	$t_{SHIFT\_MIN} – t_{DCD} – t_{IOSKEW} – t_{EXT} – t_{DS}$
	Write Hold Timing Margin	210	110	$0.5*t_{CK} – t_{SHIFT\_MAX} – t_{DCD} – t_{IOSKEW} – t_{EXT} – t_{DH}$
	Total Margin	420	220	$0.5*t_{CK} – t_{DH} – t_{DS} – 2*(t_{DCD} + t_{IOSKEW} + t_{EXT} + t_{CLKSKEW})$

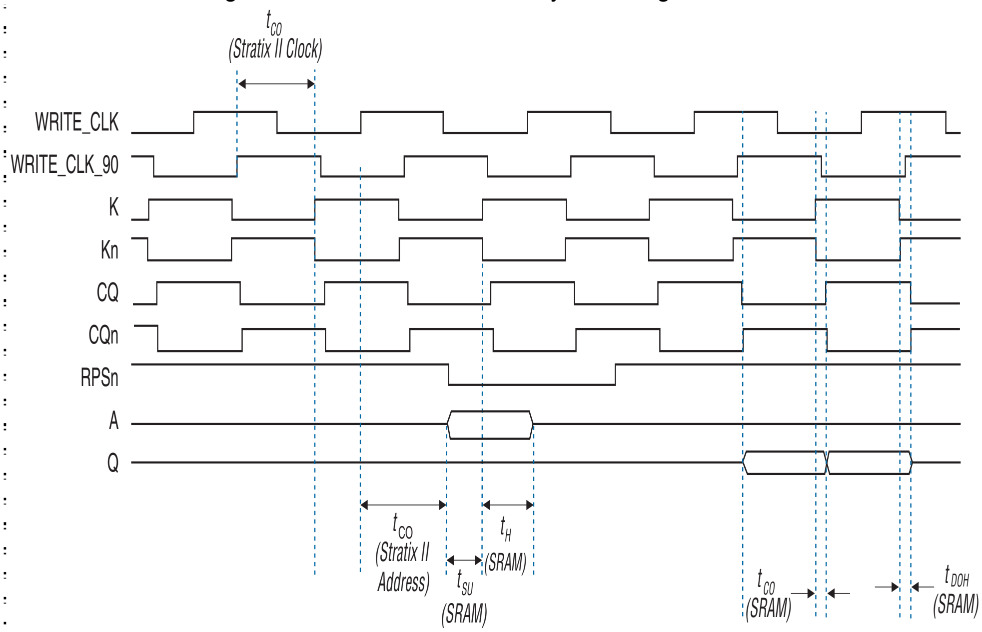
[+] Feedback

Read Cycle Timing

The FPGA controller sends the read request and address signals to the QDR-II SRAM device along with the K and Kn clocks in a similar manner to the write data. Therefore, the write timing parameters apply to these signals as well. Additionally, when the QDR-II SRAM device sends read data back to the FPGA controller, the design must meet the FPGA set-up and hold times.

Figure 8 shows the read cycle timing waveform for the QDR-II SRAM device interface pins.

Figure 8. QDR-II SRAM Read Cycle Timing Waveform



Stratix and Stratix GX Read Cycle Timing

QDR-II memory reads in Stratix and Stratix GX devices are implemented using the CQ echo clock output from the QDR-II SRAM. The CQ echo clock signal is directly fed into a PLL to centrally align the clock with the input data (Q). This is achieved by implementing a phase shift on the PLL, and using this phase-shifted clock to latch data from memory in the DDIO registers.

In the following exercise, we analyze the timing for a read operation from a Cypress CY7C1313AV18-200 burst-of-4 QDR-II SRAM device to the Stratix EP1S40 device. We will analyze timing for a 200-MHz interface.

We start the analysis by studying the relationship between the echo clocks (CQ, CQn) and read data (Q) signals from the QDR-II SRAM. Cypress data sheet specifies the data clock-to-output (tCQD) and data hold times (tCQDOH) with respect to the echo clocks. For the CY7C1313AV18-200, these timing numbers are 350 ps and –350 ps, respectively. Hence the data valid window at the QDR-II SRAM device pins is 1800 ps. Figure 9 illustrates these delays and other uncertainties in a read cycle timing waveform.

The board trace delays on the CQ/CQn signals and data bus can be ignored if the trace lengths are matched (=L2 in Figure 5). This timing analysis allows for a maximum board skew of ±50 ps between these lines. The data valid window is further reduced by this skew to 1700 ps.

The next step is to analyze the set-up and hold margins for latching the read data (Q) signals at the FPGA's DDR input pins. The echo clock, CQ, from the QDR-II SRAM is connected to the dedicated reference clock input pin of the Stratix enhanced PLL. This read PLL phase shifts the clock to centrally align the clock's edges to the data (default phase shift of 90°). Additionally, uncertainty is introduced on read clock by the PLL in the form of jitter (±100 ps).

Worst-case set-up and hold time requirements from the Stratix EP1S40 are 750 ps and –290 ps, respectively. These numbers were obtained from Quartus II timing analyzer reports. While performing timing analysis for your specific design, you obtain these requirements from the Quartus II timing analyzer as well.

Given these parameters, the set-up and hold margins for 200-MHz QDR-II in Stratix are as follows:

Set-up time margin is the least when the data arrives late and the clock arrives early. Set-up time margin is calculated as:

tsu_margin = tPLL_PS – tJITTER – tEXT – tSU – tCQD = 1.250 – 0.100 – 0.050 – 0.750 – 0.350 = 0.0 ns

[+] Feedback

Hold time margin is the least when the data arrives early and clock arrives late. The margin is calculated as:

th_margin = tCK/2 – tCQDOH – tH – tEXT – tPLL_PS – tJITTER = 2.500 – 0.350 – (–0.290) – 0.050 – 1.250 – 0.100 = 1.040 ns

The total margin available is the sum of the set-up and hold margins = 1.040 ns. Since the hold margin is larger than the set-up margin, the PLL phase shift can be adjusted to balance the margins. An additional phase shift of 0.520 ns to the existing 90° or 1.25-ns phase shift would result in equal margins. This amounts to a total real PLL phase shift of 127° on the echo clock.

Table 4 shows the QDR-II SRAM read timing margin analysis at 200 MHz when the board trace variations for the Q and CQ/CQn pins are ±50 ps (approximately 0.3” of FR4 trace length variations). A similar timing analysis can be performed for your interface with another FPGA-QDR-II SRAM device combination by replacing timing specifications in Table 4 with those from corresponding data sheets.

Figure 9. QDR-II SRAM Read Timing Waveform: Uncertainties and Margins

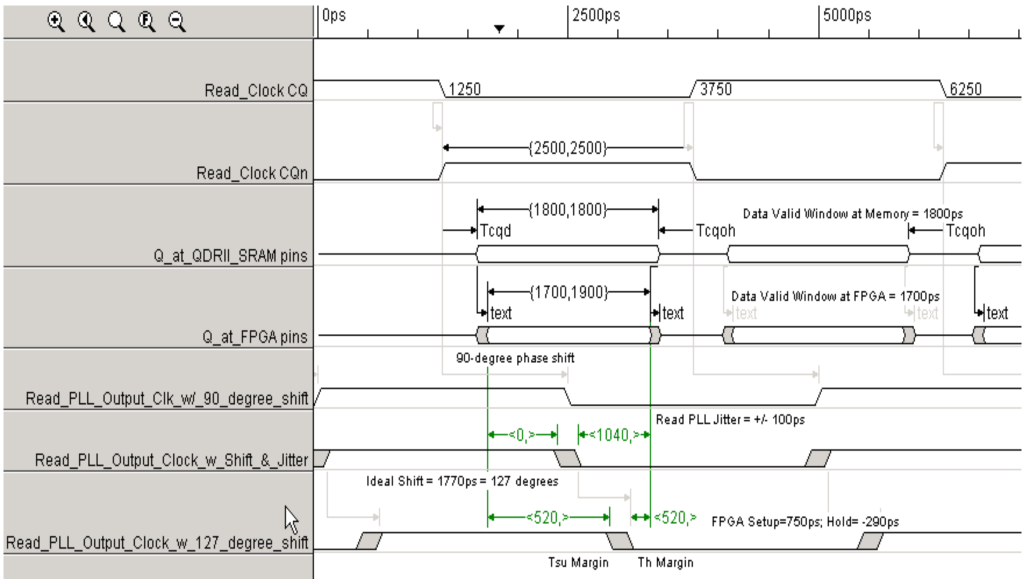


Table 4. Example Stratix EP1S40 Read Timing Analysis When Using a Read PLL

	Specification	200 MHz (ps)	Description
Memory Spec	t_{CYC}	5000	Clock Period
	t_{CQD}	350	Clock-to-out time for read data with respect to echo clock
	t_{CQDOH}	–350	Read data hold time with respect to echo clock
FPGA Spec	t_{JITTER}	±100	Stratix device read PLL jitter
	t_{PLL_PS}	1250	Default PLL phase shift for center-aligning CQ with Q = 90° = 0.25* t_{CK}
	t_{SU}	750	Data set-up time at Altera FPGA IOE register (rounded up)
	t_H	–290	Data hold time at Altera FPGA IOE register (rounded up)
Board Spec	t_{EXT}	±50	Board trace variations between the data (Q) and clock (CQ/CQn) lines

Table 4. Example Stratix EP1S40 Read Timing Analysis When Using a Read PLL (Continued)

	Specification	200 MHz (ps)	Description
Results	Data Valid Window @ FPGA input pins	1700	$t_{CK}/2 – t_{CQD} + t_{CQDOH} – 2^* t_{EXT}$
	Read set-up timing margin	0	$t_{PLL\_PS} – t_{JITTER} – t_{EXT} – t_{SU} – t_{CQD}$
	Read hold timing margin	1040	$t_{CK}/2 – t_{CQDOH} – t_H – t_{EXT} – t_{PLL\_PS} – t_{JITTER}$
	Total Margin	1040	$t_{CK}/2 – t^{CQD} + t_{CQDOH} – 2^*t_{EXT} – t_{SU} – t_H – 2^* t_{JITTER}$
	Ideal Phase Shift	1770 = 127°	Ideal Real PLL phase shift for equal set-up and hold margins = 1250 + (0+1040)/2

Table 5. Example Stratix II EP2S60 Read Timing Analysis (Using the DQS Circuitry)

	Specification	250 MHz (ps)	Description
Memory Spec	t_{CYC}	4000	Clock Period
	t_{CQD}	300	Clock-to-out time for read data with respect to echo clock
	t_{CQDOH}	–300	Read data hold time with respect to echo clock
FPGA Spec	t_{DLL_PS}	1000	Default DLL phase shift for center-aligning CQ with Q = 90° = 0.25* t_{CK}
	$t_{DLLJITTER}$	±100	Stratix device DLL Jitter
	t_{PSERR}	82	DLL Phase Shift Error
	t_{DQSINT}	150	DQS-DQ internal skew inside Stratix device
	t_{SU}	210	Data set-up time at Altera FPGA IOE register (rounded up)
	t_H	180	Data hold time at Altera FPGA IOE register (rounded up)
Board Spec	t_{EXT}	±50	Board trace variations between the data (Q) and clock (CQ/CQn) lines
Results	Data Valid Window @ FPGA input pins	1300	$t_{CK}/2 – t_{CQD} + t_{CQDOH} – 2^* t_{EXT}$
	Read set-up timing margin	108	$t_{DLL\_PS} – t_{JITTER} – t_{PSERR} – t_{DQDINT} – t_{EXT} – t_{SU} – t_{CQD}$
	Read hold timing margin	138	$t_{CK}/2 – t_{CQDOH} – t_H – t_{EXT} – t_{DLL\_PS} – t_{JITTER} – t_{PSERR} – t_{DQDINT}$
	Total Margin	246	$t_{CK}/2 – t_{CQD} + t_{CQDOH} – 2^*t_{EXT} – t_{SU} – t_H – 2^*(t_{JITTER} – t_{PSERR} – t_{DQDINT})$
	Ideal Phase Shift	1123 = 101°	Ideal Real PLL phase shift for equal set-up and hold margins = 1000 + (108 + 138)/2

Stratix II Read Cycle Timing

A similar timing analysis is performed for Stratix II devices. The main difference in the analysis is that the echo clock used to capture read data is phase shifted using a DLL instead of the PLL. Hence, the clock uncertainties are DLL jitter and clock skew to the different read input DDR circuits inside the Stratix II.

Table 5 shows the QDR-II SRAM read timing margin analysis at 250 MHz when the board trace variations for the DQ and DQS pins are 50 ps (approximately 0.3” of FR4 trace length variations). You can perform a similar timing analysis for your interface with another QDR-II SRAM device by replacing the tCO and tDOH values in Table 4 with those from the QDR-II SRAM data sheet.

Read/Write Cycle Timing

The QDR-II SRAM controller has independent read and write paths. Therefore, timing does not change for a stand-alone read or write versus a combined read/write operation.

Design Guidelines

Cypress recommends the following guidelines for QDR-II interface implementation. These guidelines are derived from QDR-II interface validation on Stratix and Stratix GX FPGAs. Recommendations for Stratix II FPGAs will be made available pending characterization.

I/O Standard and Termination

1.8V or 1.5V HSTL I/O standard with Class I termination is recommended for best performance.

Impedance Matching

The recommened value is to have 50-ohm impedance matching. If higher drive strength is needed on the outputs, minimum impedance mode can be used with termination at the far end.This will be adequate for memory interface operation at the highest supported speed for a particular device density and speed grade.

Trace Lengths

As described in previous sections, trace lengths for all read side and write side signals should be matched. Read side interface signals include the Q read data pins and CQ/CQn echo clock pins from the QDR-II SRAM. Write side interface signals include the D write data pins and K/Kn system clock pins from the FPGA (in single-clock mode).

Clamshell Configuration

QDR-II SRAM pinout supports clamshell configuration, where two QDR-II devices can be placed on either side of the printed circuit board.

Conclusion

QDR-II SRAM devices offer enhanced timing margin and flexibility over QDR SRAM devices. Designed for high-bandwidth communications, networking, and DSP applications, QDR-II SRAM devices and Altera’s Stratix II, Stratix, and Stratix GX devices help communications system designers take advantage of QDR-II SRAM technology and achieve high memory bandwidth through a simple, proven interface.

In March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-xxxxx, beginning with rev. **), located in the footer of the document, will be used in all subsequent revisions

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